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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,740	06/25/2003	Hirokuni Fujiyama	60188-618	9913

7590 07/06/2004

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,740	FUJIYAMA ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3* is/are allowed.

6)☒ Claim(s) *1,6,8 and 11* is/are rejected.

7)☒ Claim(s) *2,4,5,7,9,10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Wietecha et al. (USP 5736885).

As to claim 1, Wietcha et al. discloses in figure 1 an offset control circuit for adjusting offset voltages contained in differential voltages (VPOS, VNEG) that are input from a pair of differential voltage input terminals (gates of M5, M6) and outputting the adjusted differential voltages from a pair of differential voltage output terminals (sources of M5, M6), the offset control circuit comprising: a voltage/current converting portion (M5, M6) that includes the pair of differential voltage input terminals and a pair of differential current output terminals, that generates a pair of differential output currents corresponding to a potential difference between a pair of differential input voltages input from the pair of differential voltage input terminals, and that outputs the pair of differential output currents from the pair of differential current output terminals; an offset adjusting current-generating portion (M1, M2) that includes a pair of offset adjusting current-output terminals (drains of M1, M2) connected to the pair of differential current output terminals of the voltage/current converting portion, and at least two offset adjusting current-control terminals (gates of M1, M2), that generates a pair of offset adjusting currents by being controlled by offset adjusting current control signals (22, 24) input from the

offset adjusting current-control terminals, and that outputs the pair of offset adjusting currents from the pair of offset adjusting current-output terminals; and a current/voltage converting portion (R1) that includes a pair of differential terminals (the two ends of R1) connected to the pair of differential current output terminals of the voltage/current converting portion, the pair of offset adjusting current-output terminals of the offset adjusting current-generating portion and the pair of differential voltage output terminals, that feeds a current flowing between the two differential terminals constituting the pair of differential terminals, that converts the current into a corresponding voltage, and that generates the converted voltage at the pair of differential voltage output terminals.

As to claim 6, figure 1 shows the current/voltage converting portion is resistor means having a predetermined resistance and being connected between the pair of differential terminals.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wietecha (USP 5736885).

As to claim 8, Wietecha's figure 1 shows all limitations of the claim except for the "current/voltage converting portion is a fifth transistor that is connected between the pair of differential terminals and whose gate is connected to an input/output current control terminal". However, it is notoriously well known in the art that MOSFET that controlled by a bias voltage

is function as a resistor. Therefore, it would have been obvious to one having ordinary skill in the art to use MOSFET connected as resistor for Wietecha's resistor R1 for the purpose of saving space.

As to claim 11, figure 1 shows a processing circuit (circuit, not shown, that generating VNEG and VPOS) that performs predetermined processing for a differential output voltage(VNEG, VPOS)whose offset voltage has been adjusted with the offset control circuit (circuit figure 1). Thus, figure 1 shows all limitations of the claim except for "the offset control circuit and the processing circuit are formed on a single chip". However, it is notoriously well known in the art that circuits in the same chip have the same process of variation and temperature characteristic. Therefore, it would have been obvious to one having ordinary skill in the art to make the circuit that generating signals VNG and VPOS and circuit figure 1 in the same chip for the purpose of matching the temperature characteristic.

Allowable Subject Matter

5. Claims 2, 4, 5, 7, 9, 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claim 3 is allowed.

Claims 2, 4, 5, 7, 9 and 10 would be and claim 3 are allowable because the prior art fails to teach the voltage/current converting portion, current/voltage converting portion, and offset adjusting current generating portion having the combine of elements as claimed.

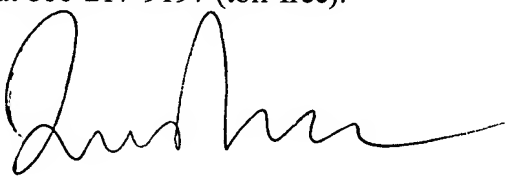
Claim 12 would be allowable because the prior art fails to teach the processing circuit having elements as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Quan Tra
Patent Examiner

July 1, 2004